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Building blocks for future dual-channel GaN gate drivers: Arbitrary waveform driver, bootstrap voltage supply, and level shifter

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Abstract—Capitalising on the high-speed switching capability of 650 V GaN FETs in power-electronic bridge-legs is challenging. Whilst active gate driving has previously been shown to help overcome adverse switching behaviour, the best results are likely to be achieved through a combination of uncompromised circuit layout and active gate driving. A fully integrated dual-channel driver would minimise external circuitry and allow power devices to be placed as close together as possible. This would facilitate simultaneous minimization of parasitic inductances in the gate-drive and power-circuit loops. Other benefits would include ease of use, lower BOM cost, and providing a step towards full integration of driver and power stage. This paper presents three circuit blocks vital to the implementation of a fully integrated dual-channel gate driver – A 100 ps resolution, digitally-controlled active gate driver IC, a sub-ns propagation delay level shifter with 200 V/ns slew-rate immunity, and a regulated bootstrap supply that maintains its output voltage regardless of any switch-node undershoot during switching events. Measurement results show the efficacy of the high-resolution active gate driver in a GaN bridge leg, and the sub-ns propagation delay of the level shifter, both fabricated in a 50 V CMOS process. Simulation results demonstrate the slew-immunity of the level shifter, and operation of the bootstrap supply. It is also inferred how to increase the voltage rating of the level-shifter and bootstrap without adversely affecting performance.

Keywords—Active gate driver, bootstrap power supply，dual-channel gate driver, level shifter, GaN

I. INTRODUCTION

The half-bridge power stage is an essential circuit block in power electronics [1]. The layout of low-EMI 650 V GaN half-bridges is challenging, and a range of solutions have been proposed. Active gate drivers, for example, have been reported to increase power efficiency and suppress EMI for a given layout, for IGBTs [2], Silicon MOSFETs [3], and SiC JFETs [4], and recently, the first inroads have been made into the active gate driving of GaN FETs [5], albeit open-loop. Since GaN devices are so small for a given current rating, the layout itself could be significantly improved by integrating the high-and low-side drivers into a dual-channel driver. This would make possible a circuit layout with reduced gate-loop and power-loop parasitic inductances. This, in turn, improves circuit performance, minimising overshoots and ringing, and allows better utilisation of the high-speed features of GaN FETs. It also permits the integration of functions that involve both power devices, such as dead-time optimisation[6].

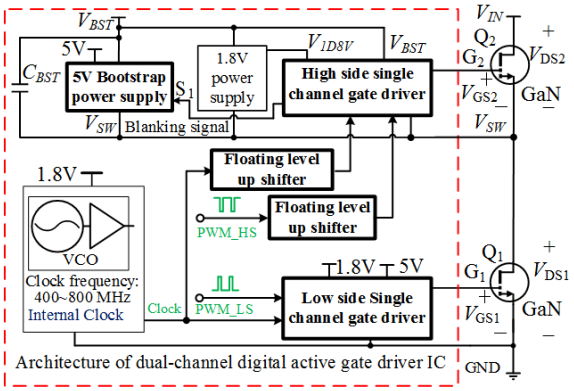

Fig.1. A possible future dual-channel digital active gate driver for GaN FETs: The sub-circuits addressed in this paper are shown in bold.

This work aims to enable future dual-channel active driver ICs for mains-voltage GaN bridge legs, as shown in Fig.1, to provide safe and quiet switching at 100 V/ns. The paper focuses on three sub-circuits of a dual-channel gate driver that are critical to permit switch-node slew rates of 100 V/ns: A new single-channel arbitrary waveform gate driver with 10 GHz update rate; a level shifter with sub-nanosecond propagation delay, 200 V/ns slew rate immunity, and potential for use in mains-voltage applications; and an accurate high-side bootstrap power supply.

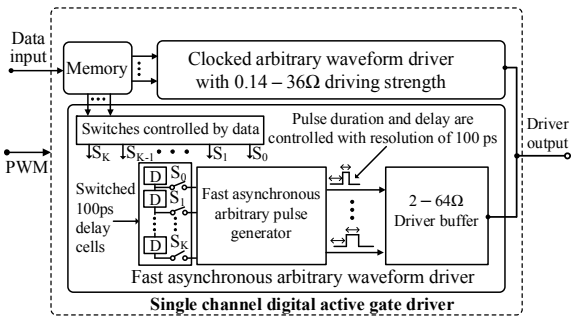

Fig.2. Architecture of the single-channel active gate driver.

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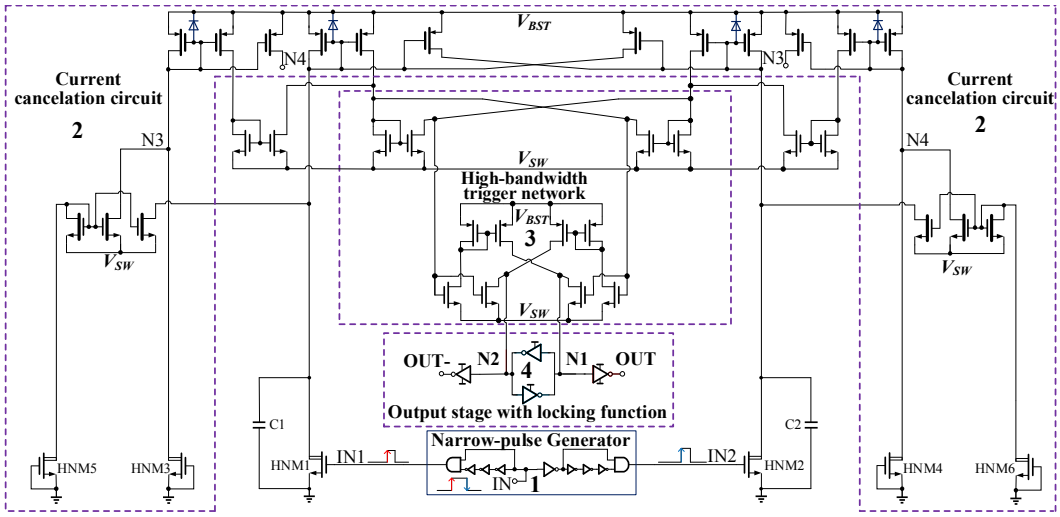

Fig.3. Schematic of level shifter, with sub-nanosecond delay, and 200 V/ns slew rate tolerance.

II. Design of Three Proposed Sub-Circuits

A. Single-channel active gate driver

The single-channel active gate driver with 100 ps driving resolution is shown in Fig. 2. The output stage is split into a slower clocked part (top) and a fast asynchronous part (bottom). The driver includes a memory whose stored data defines the driver's output impedance sequences that occur on input PWM signal transitions. The clocked arbitrary driver has 8-bit driving resolution and 0.14 Ω - 36 Ω driving strength. The driving strength is synchronously updated at a rate determined by the internal clock. The faster asynchronous arbitrary waveform driver includes an arbitrary pulse generator and a fast driver buffer. The pulse generator produces driving pulses with a 100 ps resolution, and the 6-bit fast driver buffer delivers these pulses with driving strengths of 2 Ω - 64 Ω.

On each PWM edge, a gate-drive sequence of 8 internal clock cycles' duration is read from the memory by the internal control logic. The setting in the 8th clock period is maintained until the next PWM transition, and there are independent resistance sequences for low-to-high and high-to-low transitions.

B. Floating level shifter with sub-nanosecond propagation delay and high slew rate immunity

A level shifter with short propagation delay and high slew rate immunity is a vital component for high-side GaN FET gate drivers [7]. The level shifter circuit in this work is shown in Fig. 3. The design technique is detailed in [8]. This level shifter includes 4 main blocks:

1. An input narrow-pulse generator that detects the input *IN* edges and generates the narrow trigger pulses.
2. A current cancellation circuit that prevents currents flowing through parasitic capacitors C_1 and C_2 from triggering the level shifter during positive or negative transients.
3. A high-bandwidth network that mirrors the input triggering current generated by HNM1 and HNM2 to trigger the output stage.
4. An output stage that correctly locks the output state, according to input signal *IN*.

This level shifter has been verified through a 50 V CMOS process. To apply it to a higher voltage rating bridge-leg converter, an appropriate process should be selected. In this case, devices in blocks 2, 3, and 4 would still be low-voltage devices, built in a higher isolation N-well. The propagation delay is affected only by the features of HNM1-HNM6. The 'intrinsic' delay [10] of these devices is increased with higher voltage rating, but the overall propagation delay will remain low. The slew rate tolerance is derived from the symmetric architecture with good layout matching, and we therefore anticipate it to be unaffected by the use of higher-voltage rated devices when implementing a 600 V version.

C. Accurate high-side bootstrap power supply

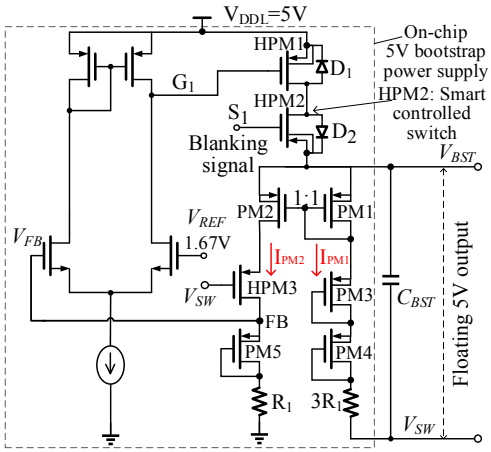

Fig.4. 5 V high-side bootstrap power supply generated from low-side 5V power supply.

The circuit of the high-side bootstrap power supply is shown in Fig. 4, and its operation illustrated in Fig. 5. The bootstrap capacitor C_{BST} is charged during the charging phase when the switch-node voltage is low (i.e., when Q_1 of Fig. 1 is on), but only after the deadtime is over, in order to protect from overcharging. To this end, HPM2 is gated with a blanking signal, Fig. 5. During this charging phase, the bootstrap voltage is regulated to 5 V, by HPM1, whose gate is controlled through the negative feedback that forces V_{FB} and V_{REF} to have the same voltage of 1.67 V. PM1 to PM5

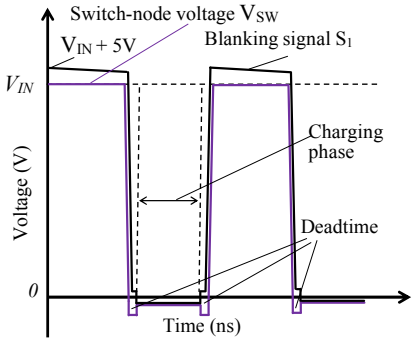

Fig.5. Control of bootstrap charging using blanking signal S_1: Switch off HPM2 outside of charging phase to protect bootstrap circuit. Switch on only after deadtime to avoid overshoot on bootstrap voltage.

have the same size and each PMOS device's bulk and source are connected together to eliminate body effect and to guarantee they have the same threshold voltage. Current mirrors composed by PM1 and PM2 make I_{PM1} and I_{PM2} equal, and gate-to-source voltages of PM1 to PM5 are equal as a result.

$$I_{PM1} = \frac{(V_{BST} - V_{SW}) - 3 * V_{GS(PM1)}}{3 * R1} \quad (1)$$

$$I_{PM2} = \frac{V_{REF} - V_{GS(PM4)}}{R1} \quad (2)$$

As $I_{PM1} = I_{PM2}$, it can be concluded:

$$V_{BST} - V_{SW} = 3 * V_{REF} = 5V \quad (3)$$

From equation (3), we conclude the voltage across C_{BST} is accurately maintained at 5 V regardless of the value of switch node voltage V_{SW} during the charging phase. Outside of the charging phase, the blanking signal S_1 is set to equal V_{BST} to turn off HPM2, and HPM2 blocks the high voltage when V_{SW} is equal to the bridge-leg DC link V_{IN}. HPM3 protects the source of PM4 when V_{SW} equals V_{IN}.

The charging phase operates with $V_{DDL} = 5V$ regardless of process choice. For a 600 V implementation, PM1-PM5 need to be placed in the 600 V isolation well. The parasitic diode D2 must block 600 V. HPM3 also needs to be a 600 V device to protect node *FB*, which sits at around 1.67 V.

III. Measurement and Simulation Results

The single-channel active gate driver is fabricated on an AMS 50 V HV CMOS process, occupying 5 mm^2. It is

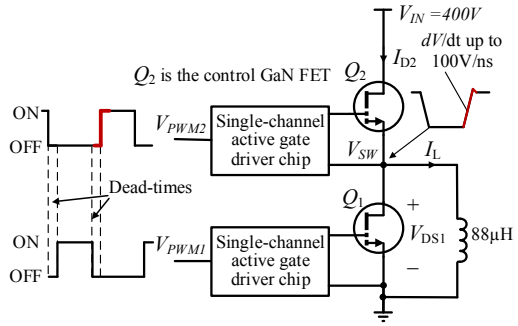

Fig.6. Measurement setup: Bridge-leg Buck converter with two GS66508P GaN FETs, each driven by one single-channel active gate driver IC.

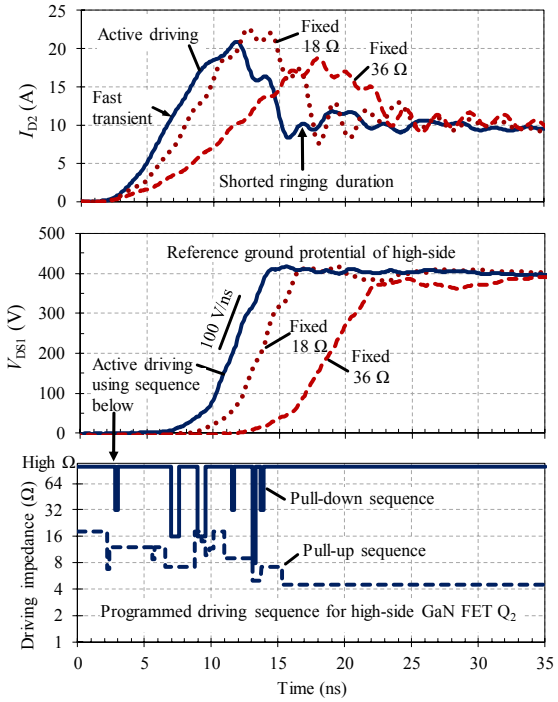

Fig.7. Demonstration of high-side driver actively controlling the upper device to shape the drain current, whilst its ground reference VDS1 is slewing at 100 V/ns. The resulting current switches faster with a significantly reduced ringing duration.

demonstrated experimentally on the high-side of the bridge leg Buck converter of Fig. 6, to validate its performance under fast slewing. Measured results for turn-on are given in Fig. 7. The drain current I_{D2} is measured using an Infinity Sensor [9] that has just 0.2 nH insertion inductance. The measurement results are shown to correctly output 100-ps-resolution, pre-programmed driving sequences, whilst the switch-node V_{SW} is slewing at 100 V/ns. This is, in part, enabled by use of TI's digital isolators (ISO78x) with a CMTI of 100 V/ns. Active driving is seen to reduce the duration of current ringing by more than half, as well as peak overshoot, whilst simultaneously speeding up the switching transient, when compared to driving with a fixed 18 Ω gate resistance. This improvement in the current overshoot behaviour is not possible by simply adding gate resistance; this is illustrated by the result using a fixed 36 Ω gate resistance: Here the switching losses are high, and yet the ringing is still present.

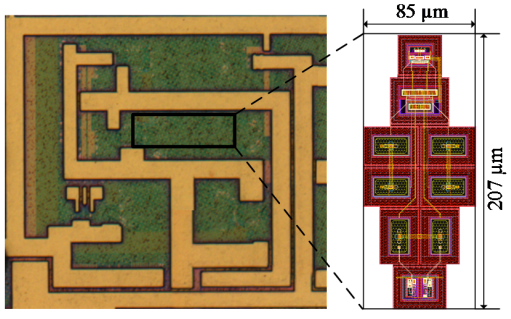

Fig.8. Die photo of level shifter.

The proposed signal level-shifting circuit is also fabricated with AMS 50 V HV CMOS process. Its micrograph photo is shown in Fig. 8. Fig. 9 shows the measurement result of propagation delay that is below 750 ps with V_{SW} up to 45 V.

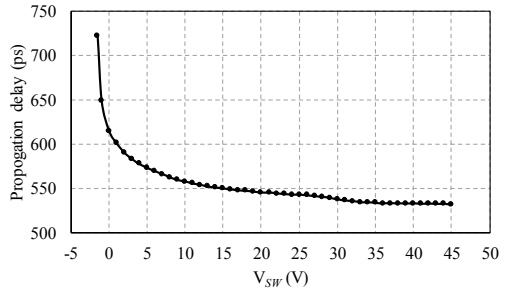

Fig.9. Measured propagation delay of the level shifter.

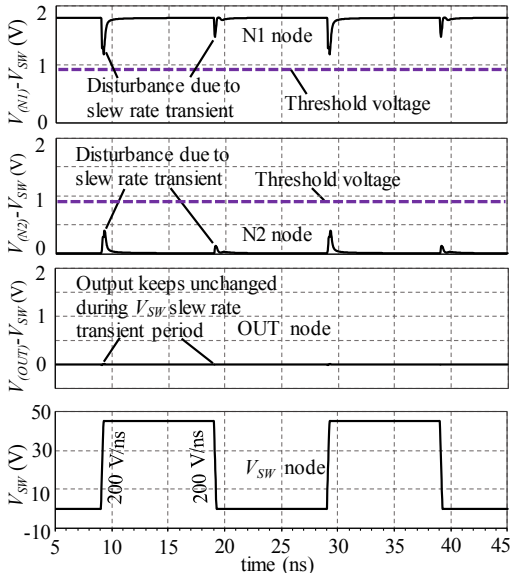

Fig. 10: Post-layout simulation showing that the level shifter is immune to switch-node slew-rates up to 200 V/ns.

Post-layout simulation results in Fig. 10 show that the level shifter is immune to 200 V/ns slewing of the switch node voltage.

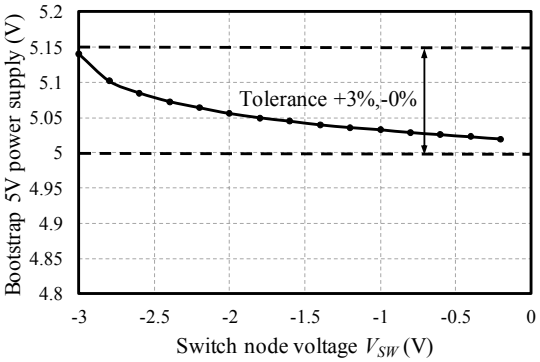

Fig.11. Bootstrap 5V power supply is independent of negative switch node V_{SW} voltage during charging phase (low-side GaN FET is on and reverse conducting).

The performance of the bootstrap power supply is demonstrated by simulation in Fig. 11. The supply maintains an output of between 5.14 V and 5.05 V during the charging phase, independent of the high-side reference potential, which is typically around -0.5 V during synchronous conduction, and -2 V during the dead time.

IV. Conclusion

Three key circuit blocks required to realise a fully integrated dual-channel active gate driver for GaN FETs have been presented: a single-channel active gate driver, a level shifter, and an accurate 5 V bootstrap power supply. The single-channel active gate driver and level shifter are fabricated with the AMS 50 V HV CMOS process and verified through measurements. The simulation results of the charging phase characteristic of the bootstrap power supply demonstrate reliable operation in the face of switch-node voltage undershoots. For the implementation for mains-voltage bridge-legs with 400 V DC links, an alternative process is required to give the required blocking capability to the level shifter and bootstrap supply [11]. It is noted which devices would have to support the additional voltage, and how circuit operation would be affected by these changes.

The presented circuit blocks could also be used to realise a fully-integrated power stage that includes the gate drivers and both power devices. The arbitrary waveform gate driver is particularly attractive here as it offers system designers full flexibility to tune the behaviour of the gate driver whilst eliminating the most challenging aspects of circuit layout.

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